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(71) Applicant *(for all designated States except US)*: **KABUSHIKI KAISHA TOSHIBA** [JP/JP]; 1-1, Shibaura 1-chome, Minato-ku, Tokyo 105-8001 (JP).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **TODA, Haruki** [JP/JP]; 105,111-1, Nishitakenomaru, Naka-ku, Yokohama-shi, Kanagawa 231-0852 (JP).

(74) Agent: **ITAMI, Masaru**; 301, Daini-Seikoh Bldg., 2-11, Kudan-kita 4-chome, Chiyoda-ku, Tokyo 102-0073 (JP).

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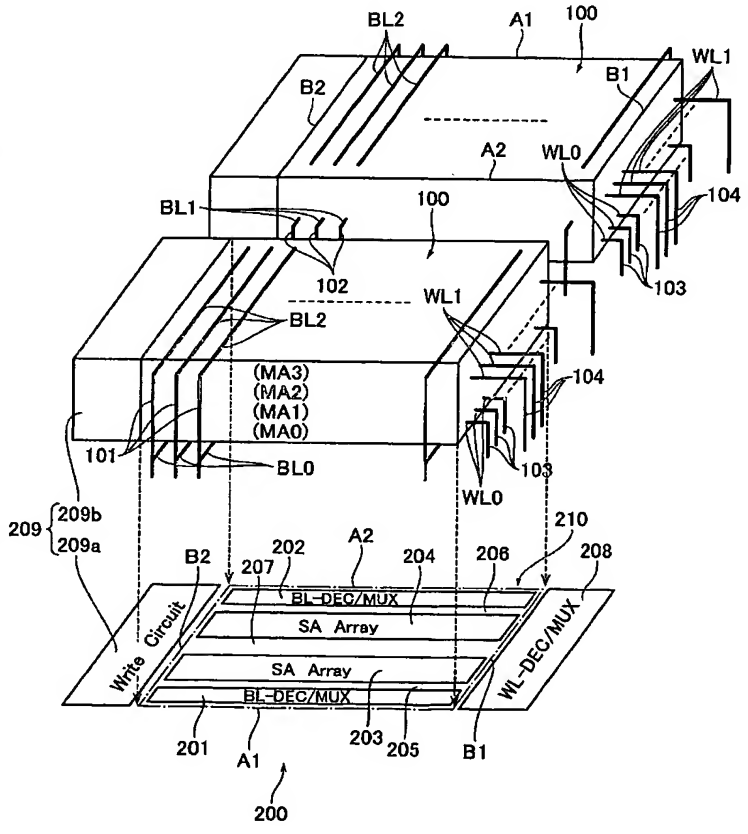
(54) Title: PHASE CHANGE MEMORY DEVICE



(57) Abstract: A phase change memory device has a semiconductor substrate; a plurality of cell arrays stacked above the semiconductor substrate, each cell array having memory cells arranged in a matrix manner for storing resistance values as data that are determined by phase change of the memory cells, bit lines each commonly connecting one ends of plural memory cells arranged along a first direction of the matrix and word lines each commonly connecting the other ends of plural memory cells arranged along a second direction of the matrix; a read/write circuit formed on the semiconductor substrate as underlying the cell arrays for reading and writing data of the cell arrays; first and second vertical wirings disposed outside of first and second boundaries that define a cell layout region of the cell arrays in the first direction to connect the bit lines of the respective cell arrays to the read/write circuit; and third vertical wirings disposed outside of one of third and fourth boundaries that define the cell layout region in the second direction to connect the word lines of the respective cell arrays to the read/write circuit.

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